EO/US PTO-1390 (Modified) (REV 11-2000) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U S APPLICATION NO (IF KNOWN, SEE 37 CFR
521.1014	10/070032

INTERNATIONAL APPLICATION NO	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP00/01745	1 March 2000	19 April 1999

TITLE OF INVENTION
DATA TRANSMISSION DEVICE

APPLICANT(S) FOR DO/EO/US
Horea-Stefan CULCA

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S C 371
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U S C 371
3. ☒ This is an express request to begin national examination procedures (35 U S C 371(f)). The submission must include items (5), (6), (9) and (24) indicated below
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31)
5. ☒ A copy of the International Application as filed (35 U S C 371 (c) (2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau)
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ An English language translation of the International Application as filed (35 U.S C. 371(c)(2)).
   a. ☒ is attached hereto
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4)
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau)
   b. ☐ have been communicated by the International Bureau
   c. ☐ have not been made, however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U S.C. 371(c)(3))
9. ☒ An oath or declaration of the inventor(s) (35 U S C 371 (c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U S C 371 (c)(5))
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409)
12. ☒ A copy of the International Search Report (PCT/ISA/210)

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1 97 and 1 98
14. ☐ An assignment document for recording A separate cover sheet in compliance with 37 CFR 3 28 and 3 31 is included
15. ☒ A **FIRST** preliminary amendment
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment
17. ☐ A substitute specification
18. ☐ A change of power of attorney and/or address letter
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter 2 and 35 U S C 1 821 - 1 825
20. ☐ A second copy of the published international application under 35 U S C 154(d)(4)
21. ☐ A second copy of the English language translation of the international application under 35 U S C 154(d)(4)
22. ☐ Certificate of Mailing by Express Mail
23. ☐ Other items or information

Letter re: Priority

APPLICATION NO (IF KNOWN, SEE 37 CFR	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
	PCT/EP00/01745	521.1014

24. The following fees are submitted

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1 482) nor international search fee (37 CFR 1 445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO	$1040.00
☒	International preliminary examination fee (37 CFR 1 482) not paid to USPTO but International Search Report prepared by the EPO or JPO	$890.00
☐	International preliminary examination fee (37 CFR 1 482) not paid to USPTO but international search fee (37 CFR 1 445(a)(2)) paid to USPTO .	$740.00
☐	International preliminary examination fee (37 CFR 1 482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) . .	$710.00
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) . . .	$100.00

ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1 492 (e))	$0.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	4 - 20 =	0	x $18 00	$0.00	
Independent claims	2 - 3 =	0	x $84 00	$0.00	
Multiple Dependent Claims **(check if applicable)**			☐	$0.00	
TOTAL OF ABOVE CALCULATIONS =				$890.00	
☐ Applicant claims small entity status See 37 CFR 1 27). The fees indicated above are reduced by 1/2				$0.00	
SUBTOTAL =				$890.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1 492 (f)). +				$0.00	
TOTAL NATIONAL FEE =				$890.00	
Fee for recording the enclosed assignment (37 CFR 1 21(h)) The assignment must be accompanied by an appropriate cover sheet (37 CFR 3 28, 3.31) **(check if applicable).** ☐				$0.00	
TOTAL FEES ENCLOSED =				$890.00	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of **$890.00** to cover the above fees is enclosed

b. ☐ Please charge my Deposit Account No _____ in the amount of _____ to cover the above fees
A duplicate copy of this sheet is enclosed

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No **50-0552** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card **WARNING:** Information on this form may become public **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO

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23280
PATENT TRADEMARK OFFICE

SIGNATURE

Robert J. Paradiso
NAME

41,240
REGISTRATION NUMBER

October 18, 2001
DATE

[521.1014]

UNITED STATES PATENT AND TRADEMARK OFFICE

Re:	Application of:	Horea-Stefan CULCA
	Serial No.:	To Be Assigned
	International Application No.:	PCT/EP00/01745
	Filed:	Herewith
	For:	DATA TRANSMISSION DEVICE

BOX PCT
Asst. Commissioner for Patents
Washington, D.C. 20231

October 18, 2001

PRELIMINARY AMENDMENT

Sir:

Applicants request that the following Amendments be made in the above-identified matter prior to examination thereof:

IN THE SPECIFICATION

Before paragraph [0001], please insert the heading --BACKGROUND--.

Please amend paragraph [0001] as follows:

[0001] The present invention relates to a data transmission device having a master device and a slave device connected via at least one data transmission line and one clock signal line.

Page 2, before paragraph [0009] please insert the heading --SUMMARY OF THE INVENTION--.

Please amend paragraph [0009] as follows:

[0009] Therefore, an object of the present invention is to provide a data transmission device which, in a simple way, offers increased interference immunity in a serial data transmission.

Page 2, please insert paragraph [0009.1] as follows:

--[0009.1] The present invention provides a data transmission device for serial synchronous data transmission. The data transmission device includes a master device including a first arithmetic unit and a master interface and a slave device including a second arithmetic unit and a slave interface. The master and slave interfaces are capable of being connected via at least one data transmission line and a clock signal line, and are capable of being connected via a acknowledgment signal line configured for a transmission of an acknowledgment signal from the slave device to the master device. The second arithmetic unit is capable of generating the acknowledgment signal upon completion of a data reading operation. The first arithmetic unit is configured so that the master device is capable of initiating a further write operation to the slave device only upon receiving the acknowledgment signal from the slave device.--.

Please delete paragraph [0010].

Before paragraph [0012], please insert the heading --BRIEF DESCRIPTION OF THE DRAWINGS--.

Please amend paragraph [0012] as follows:

[0012] Further details and advantages of the present invention will become apparent in the following description based on an exemplary embodiment, with reference to the drawings.

Before paragraph [0014], please insert the heading --DETAILED DESCRIPTION--.

Please amend paragraph [0018] as follows:

[0018] The present invention is not limited to the specific embodiments described above but is intended to be limited only by the scope of the claims appended hereto. The present invention further includes a slave device 4 which features a slave interface 24 having an acknowledgment terminal (RDY) and which contains an arithmetic unit (microprocessor or controller) which is designed in such a manner that an acknowledgment signal for master device 2 can be generated at the acknowledgment terminal (RDY) of slave interface 24 upon completion of a data reading operation. The present invention moreover includes a master device 2 which features a master interface 22 having an acknowledgment terminal (N-READY) and which includes an arithmetic unit which is designed in such a manner that a further write operation to slave device 4 can be initiated upon receipt of an acknowledgment signal from slave device 4.

Page 10, first line change "What is claimed is" to --WHAT IS CLAIMED IS--.

IN THE CLAIMS:

Please cancel claims 1-3 as presented in the underlying International Application No. PCT/EP00/01745 and cancel additional claim 4 annexed to the International Preliminary Examination Report, and add new claims 5-8 as follows:

--5. (new) A data transmission device for serial synchronous data transmission comprising:

a master device including a first arithmetic unit and a master interface; and

a slave device including a second arithmetic unit and a slave interface;

wherein:

the master and slave interfaces are capable of being connected via at least one data transmission line and a clock signal line;

the master and the slave interfaces are capable of being connected via a acknowledgment signal line configured for a transmission of an acknowledgment signal from the slave device to the master device;

the second arithmetic unit is capable of generating the acknowledgment signal upon completion of a data reading operation; and

the first arithmetic unit is configured so that a capability of the master device to initiate a further write operation to the slave device is dependent upon a receiving of the acknowledgment signal from the slave device.

6. (new) The data transmission device as recited in claim 5 wherein the at least one data transmission line is a single bidirectional data transmission line.

7. (new) The data transmission device as recited in claim 5 wherein the at least one data transmission line includes a first and a second unidirectional data transmission line.

8. (new) A method for serial synchronous data transmission in a data transmission device including a master device and a slave device, the master device including a first arithmetic unit and a master interface, the slave device including a second arithmetic unit and a slave interface, the master and slave interfaces being connected via a first and a second unidirectional data

transmission line, an acknowledgment signal line, and a clock signal line, the method comprising:

initiating, using the master device, a communication by transmitting a first transmit bit;

receiving, using the slave device, the first transmit bit after a first master-slave transmission delay;

activating, using the master device, the clock signal after a first clock signal delay time;

receiving, using the slave device, an interrupt signal from the clock signal line after a second master-slave transmission delay;

transmitting, using the slave device, a first receive bit; and

reading, using the slave device, the first transmit bit while applying a first interference suppression measure;

receiving, using the master device, the first receive bit after a first slave-master transmission delay;

activating, using the slave device, a first acknowledgment signal after a first delay time;

receiving, using the master device, the first acknowledgment signal after a second slave-master transmission delay;

deactivating, using the master device, the clock signal;

initiating, using the master device, a new cycle by transmitting a second transmit bit;

reading, using the master device, the first receive bit while applying a second interference suppression measure;

receiving, using the slave device, the second transmit bit and a first deactivated clock signal after a third master-slave transmission delay;

activating, using the master device, the clock signal after a second clock signal delay time;

deactivating, using the master device, the first acknowledgment signal after a third slave-master transmission delay;

receiving, using the slave device, a first active clock signal after a fourth master-slave transmission delay;

transmitting, using the slave device, a second receive bit;

reading, using the slave device, the second transmit bit while applying a third interference suppression measure;

receiving, using the master device, the second receive bit after a fourth slave-master transmission delay;

activating, using the slave device, a second acknowledgment signal after a second delay time;

receiving, using the master device, the second acknowledgment signal after a fifth slave-master transmission delay;

deactivating, using the master device, the clock signal;

transmitting, using the master device, a third transmit bit;

reading, using the master device, the second receive bit while applying a fourth interference suppression measure;

initiating, using the master device, a last cycle by:

transmitting a last transmit bit;

deactivating the clock signal; and

reading a receive bit of a previous cycle while applying a fifth interference suppression measure;

receiving, using the slave device, a last transmit bit and a second deactivated clock signal after a fourth master-slave transmission delay;

activating, using the master device, the clock signal after a third clock signal delay time;

deactivating, using the master device, a third acknowledgment signal after a sixth slave-master transmission delay;

receiving, using the slave device, a second active clock signal after a fifth master-slave transmission delay;

transmitting, using the slave device, a last receive bit;

reading, using the slave device, the last transmit bit while applying a sixth interference suppression measure;

receiving, using the master device, the last receive bit after a seventh slave-master transmission delay;

activating, using the slave device, a fourth acknowledgment signal after a third delay time;

receiving, using the master device, the fourth acknowledgment signal after an eighth slave-master transmission delay;

setting, using the master device, the clock signal to an inactive resting level;

reading, using the master device, the last receive bit while applying a seventh interference suppression measure;

setting, using the slave device, the first unidirectional data transmission line inactive after a sixth master-slave transmission delay;

deactivating, using the master device, the clock signal after the reading the last receive bit;

deactivating, using the slave device, a third active clock signal after a seventh master-slave transmission delay; and

deactivating, using the master device, a fifth acknowledgment signal after a ninth slave-master transmission delay.--.

IN THE ABSTRACT:

Please replace the abstract of record with the following new abstract:

--A data transmission device for serial, synchronous transmission of data includes a master device and a slave device which can be linked by at least one data transmission line and a clock signal line. The master and slave devices can be linked by an additional ready signal line for transmitting a ready signal from the slave device to the master device. When the slave device has completed a data reading operation, a ready signal can be generated for the master device. The master device is able to initiate a further writing operation to the slave device only after receiving the ready signal from the slave device. Suppression of interference by the slave device may be enhanced.--.

REMARKS

It is respectfully submitted that no new matter has been added.

Applicants believe that no fees are due as a result of this amendment. In the event of a fee discrepancy, please charge our Deposit Account No. 50-0552.

Respectfully submitted,

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Date of deposit October 18, 2001
I hereby certify that this correspondence and/or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1 10 on the date indicated above in an envelope addressed to "Commissioner of Patents and Trademarks, Washington, DC 20231"

DAVIDSON, DAVIDSON & KAPPEL, LLC

BY: _____
Samuel Gomez

Application of: Horea-Stefan CUCLA [521.1014]
International Application No. PCT/EP00/01745
Filed Herewith

VERSION OF SPECIFICATION AND CLAIMS AMENDMENTS
WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 1, paragraph [0001]:
[0001] The present invention relates to a data transmission device [according to the definition of the species in Claim 1] having a master device and a slave device connected via at least one data transmission line and one clock signal line.

Page 2, paragraph [0009]:
[0009] Therefore, [the] an object of the present invention is to provide a data transmission device which, [by simple means] in a simple way, offers [significantly increases the] increased interference immunity in a serial data transmission.

Page 3, paragraph [0012]:
[0012] Further details and advantages of the present invention [ensue from the following exemplary embodiment which will be explained in the following on the basis of Figures] will become apparent in the following description based on an exemplary embodiment, with reference to the drawings.

Page 3, paragraph [0018]:
[0018] The present invention is not limited to the specific embodiments described above but [includes all equally acting embodiments along the lines of the present invention] is intended to be limited only by the scope of the claims appended hereto. The present invention further

includes a slave device 4 which features a slave interface 24 having an acknowledgment terminal (RDY) and which contains an arithmetic unit (microprocessor or controller) which is designed in such a manner that an acknowledgment signal for master device 2 can be generated at the acknowledgment terminal (RDY) of slave interface 24 upon completion of a data reading operation. The present invention moreover includes a master device 2 which features a master interface 22 having an acknowledgment terminal (N-READY) and which [contains] includes an arithmetic unit which is designed in such a manner that a further write operation to slave device 4 can be initiated upon receipt of an acknowledgment signal from slave device 4.

Page 10 first line : --WHAT IS CLAIMED IS-- [What is claimed is].

DATA TRANSMISSION DEVICE

[0001] The present invention relates to a data transmission device according to the definition of the species in Claim 1.

[0002] Data transmission devices of the type mentioned at the outset are used today in many electrical devices. The data exchange, for instance, between different electrical switching devices gains more and more importance.

[0003] Information on programs and functions to be executed and on the devices themselves or on current device states are to be interrogatable at any time by any device at any place, and to be exchangeable among the devices. To this end, the devices are equipped down to the lowest functional levels with intelligence and corresponding device interfaces for the data exchange.

[0004] In the low-cost area, it is preferred to use serial data transmission types. This has the advantage that fewer signal lines are needed than in the case of a parallel data transmission. To keep the outlay of required hardware as low as possible, the data transmission should be implemented synchronously.

[0005] A serial synchronous data transmission between two stations requires at least one data line for bidirectional data transmission and one clock signal line or two data lines for unidirectional data transmission and one clock signal line. The clock signal line, which controls the entire signal flow between the stations, is of particular importance here. This clock signal is generated by a master device. A slave device which communicates with the master device has to adapt itself to this predetermined clock.

[0006] Known interfaces for these serial synchronous transmission types include: I^2C (Philips), SPI (Motorola), Microwire (National Semiconductor), or the like. These interfaces are generally used for the data transmission between different components within one device.

[0007] If the intention is to implement such a serial synchronous data transmission between individual devices, measures have to be taken with respect to possibly occurring interference signals. To protect, in particular, the clock signal line from interference effects, provision is usually made for hardware interference suppression measures in the form of filters and screenings. In some cases, the interference immunity is supported by additional software interference suppression measures. Such software interference suppression measures are generally implemented via a repeated reading of the received information. To this end, the information is repeatedly read at intervals of about 5 to 20 µs (average duration of the interference effects) and evaluated via a majority decision (signals which are read in the majority of cases are rated as correct). To increase the interference immunity in this kind of interference suppression, the number of read operations is increased.

[0008] Interference suppression via hardware involves the disadvantage of a relatively large expenditure for hardware. Furthermore, digital software interference suppression is insufficient since only the master device which, in fact, generates the clock signal, is able to perform repeated read operations by delaying or halting the clock signal for the required (check) read time.

[0009] Therefore, the object of the present invention is to provide a data transmission device which, by simple means, significantly increases the interference immunity in a serial data transmission.

[0010] On the basis of a data transmission device of the type mentioned at the outset, this objective is achieved according to the present invention by the characterizing features of the independent claim while advantageous refinements of the present invention can be gathered from the dependent claims.

[0011] According to the present invention, the additional acknowledgment line enables the slave device to inform the master device of the receipt of the transmitted data and that the processing of the data as well as the corresponding interference suppression

measure have been completed. The master device will not initiate any new operation in which this slave is involved until it has received the acknowledgment signal from the slave device. Due to this embodiment according to the present invention, the slave device has also the possibility to eliminate interference from received signals during an adequate period of time.

[0012] Further details and advantages of the present invention ensue from the following exemplary embodiment which will be explained in the following on the basis of Figures.

[0013] Figure 1 is a schematic representation of a data transmission device according to the present invention, including a master device and a slave device; and

Figure 2 shows a transmission protocol for the serial synchronous data transmission between two stations according to Figure 1.

[0014] Fig. 1 shows a device arrangement composed of a master device 2 and a slave device 4 which are interconnected via their data transmission interfaces, master interface 22 and slave interface 24, for the purpose of data exchange. For the purpose of communication, both devices possess an intelligence in the form of a separate arithmetic unit (for example, a microprocessor or a controller).

[0015] In a preferred embodiment, there exist at least one data transmission line (Data-Out) for transmitting data from the master to the slave device 2, 4, one data transmission line (Data-In) for transmitting data from the slave to the master device 4, 2, one clock signal line (Clock), and one acknowledgment line (Ready) according to the present invention for transmitting an acknowledgment signal from the slave to the master device 4, 2. The interfaces of the master and slave devices 2, 4 have corresponding terminal contacts, the signal inputs of master device 2 preferably being inverted in the exemplary embodiment shown. If only one data transmission line or only one data transmission connection exists for each station, this data transmission line or

connection must be suitable for bidirectional operation. In the exemplary embodiment shown, two data transmission lines (Data-Out, Data-In) exist. These are data transmission lines for a unidirectional operation; thus, an unwanted superimposition of data during simultaneous transmission of data of the two stations can be ruled out. By the implementation of an acknowledgment signal line (Ready) according to the present invention, slave device 4 is now able to inform master device 2 that the processing of received data and the checking thereof (via an interference suppression measure such as repeated reading and subsequent majority decision) is completed and slave device 4 is now ready to receive further data. Consequently, master device 2 will not initiate any new operation (in which active slave device 4 would be involved) until it receives the acknowledgment via the ready signal from slave device 4. In this manner, slave device 4 is also able to eliminate interference from signals over an adequate period of time.

[0016] In the following, the transmission protocol for the serial synchronous communication between master and slave devices 2, 4 will be explained with reference to Figure 2.

[0017] In the following description and in Figure 2, the signals will be denoted by the respective terminal designations of the interfaces of the master and slave devices. In the exemplary embodiment represented and described, the signals N-DOUT, N-CLOCK, N-DIN, N-READY of the master are inverted signals (active low).

Instant	Master	Slave
1	initiates the communication (the first cycle) by placing the first transmit bit (SBit 1) on the N-DOUT line	
2		receives SBit 1 as DATAIN after the corresponding master-slave transmission delay Tms
3	activates the N-CLOCK after the required clock delay Tdc	

4		after the transmission time Tms, the slaves receives an interrupt from the CLK line. Thereupon, it takes the following measures: a) places the first receive bit (RBit 1) on DATAOUT b) reads SBit1 from line DATAIN with interference suppression (repeated reading and comparing). If necessary, the interference suppression is carried out longer which can result in an extension of the Tdr delay.
5	receives RBit 1 after the slave-maser transmission delay Tsm	
6		activates the RDY line after the required Tdr delay
7	receives the N-READY signal after the transmission delay Tsm, and: a) deactivates the N-CLOCK signal b) places the next S-Bit on N-DOUT (initiates a new cycle) c) reads RBit1 from line N-DIN with interference suppression (repeated reading and comparing). If necessary, the interference suppression is carried out longer which can result in an extension of the Tdc delay.	
Instant 8	Master	Slave receives S-Bit 2 as DATAIN after the corresponding master-slave transmission delay Tms and deactivates the CLK

		signal; consequently deactivates RDY as well
9	activates the N-CLOCK signal after the required clock delay Tdc (can be extended due to interference-suppressed reading)	
10	N-READY becomes inactive after the transmission delay Tsm	
11		receives the activated CLK signal after the transmission delay Tms, and: a) places the next R-Bit on DATAOUT b) reads the S-Bit from line DATAIN with interference suppression (repeated reading and comparing). If necessary, the interference suppression is carried out longer which can result in an extension of the Tdr delay.
12	after the transmission delay Tsm, the RBit arrives	
13		activates RDY after the required Ready delay Tdr (can be extended due to interference-suppressed reading)
14	receives the N-READY signal after the transmission delay Tsm, and: a) deactivates the N-CLOCK signal b) places the next SBit on N-DOUT (initiates the next cycle) c) reads with interference suppression ...	
...	steps 7 -- 13 are repeated until the penultimate cycle	in this manner, bits 2 ... n-1 are transmitted
15	initiates the last cycle by placing the last transmit bit (SBit n) on the N-DOUT line. Deactivates N-CLOCK and reads the RBit n-1 with interference	

	suppression	
Instant 16	Master	Slave receives S-Bit n on DATAIN and the deactivated CLK signal after the corresponding master-slave transmission delay Tms; consequently, deactivates RDY as well
17	activates N–CLOCK after the required clock delay Tdc (can be extended due to interference-suppressed reading)	
18	N-READY becomes inactive after the transmission delay Tsm	
19		receives the activated CLK signal after the transmission delay Tms, and: a) places the last RBit n on DATAOUT b) reads the last S-Bit n from line DATAIN with interference suppression (repeated reading and comparing). If necessary, the interference suppression is carried out longer which can result in an extension of the Tdr delay.
20	receives the RBit n after the transmission delay Tsm	
21		activates RDY after the required Ready delay Tdr (can be extended due to interference-suppressed reading)
22	receives the N-READY signal after the transmission delay Tsm, and: a) sets line N-DOUT to the resting level ('high') c) reads R-Bit1 from line N-DIN with interference suppression (repeated	

	reading and comparing). If necessary, the interference suppression is carried out longer which can result in an extension of the Tdc delay (!N-CLOCK is not yet deactivated)	
23		after the transmission delay Tms, line DATAIN becomes inactive ('low')
Instant 24	Master After RBIT n is read, CLOCK is deactivated; consequently, the slave is informed of the completion of the RBIT n read operation; in this case, Tdc covers only the interference-suppressed reading and can therefore be shorter than at other times	Slave
25		After the transmission delay Tms, CLK becomes inactive; consequently, RDY is deactivated and line DATAOUT is set free ('low')
26	after the transmission delay Tsm, N-READY becomes inactive and N-DN becomes free ('high'). The master can now start the transmission of a new message.	

Tdc: clock delay at the master device

Tdr: delay of the acknowledgment signal "RDY" at the slave device

Tms: delay of the signals during the transmission from the master to the slave device

Tsm: delay of the signals during the transmission from the slave to the master device

[0018] The present invention is not limited to the specific embodiments described above but includes all equally acting embodiments along the lines of the present invention. The

present invention further includes a slave device 4 which features a slave interface 24 having an acknowledgment terminal (RDY) and which contains an arithmetic unit (microprocessor or controller) which is designed in such a manner that an acknowledgment signal for master device 2 can be generated at the acknowledgment terminal (RDY) of slave interface 24 upon completion of a data reading operation. The present invention moreover includes a master device 2 which features a master interface 22 having an acknowledgment terminal (N-READY) and which contains an arithmetic unit which is designed in such a manner that a further write operation to slave device 4 can be initiated upon receipt of an acknowledgment signal from slave device 4.

What is claimed is:

1. A data transmission device for serial synchronous data transmission,
- which features a master device (2) including an arithmetic unit and a master interface (22), and
- which contains a slave device (4) including an arithmetic unit and a slave interface (24),
- it being possible for the master and slave interfaces (22, 24) to be connected via at least one data transmission line and one clock signal line,
wherein
- the master and the slave interfaces (22, 24) are designed in such a manner that they can be connected via an additional acknowledgment signal line (Ready) for the transmission of an acknowledgment signal from the slave to the master device (24, 22);
- the arithmetic unit of the slave device (24) is designed in such a manner that the acknowledgment signal for the master device (2) can be generated upon completion of a data reading operation;
- the arithmetic unit of the master device (22) is designed in such a manner that the master device (2) can initiate a further write operation to the slave device (4) only upon receipt of the acknowledgment signal from the slave device (4).

2. The data transmission device as recited in Claim 1,
wherein exactly one bidirectional data transmission line exists.

3. The data transmission device as recited in Claim 1,
wherein two unidirectional data transmission lines (Data-Out, Data-In) exist.

Abstract

The invention relates to a data transmission device for the serial, synchronous transmission of data, comprising a master device (2) and a slave device (4) which can be linked by at least one data transmission line and a clock signal line. According to the invention, the devices can be linked by an additional ready signal line (Ready) for transmitting a ready signal from the slave device to the master device (4, 2). When the slave device (4) has completed a data reading operation, a ready signal can be generated for the master device (2). The master device is only able to initiate a further writing operation to the slave device (4) after receiving the ready signal from said slave device (4). This guarantees optimal suppression of interference by the slave device.

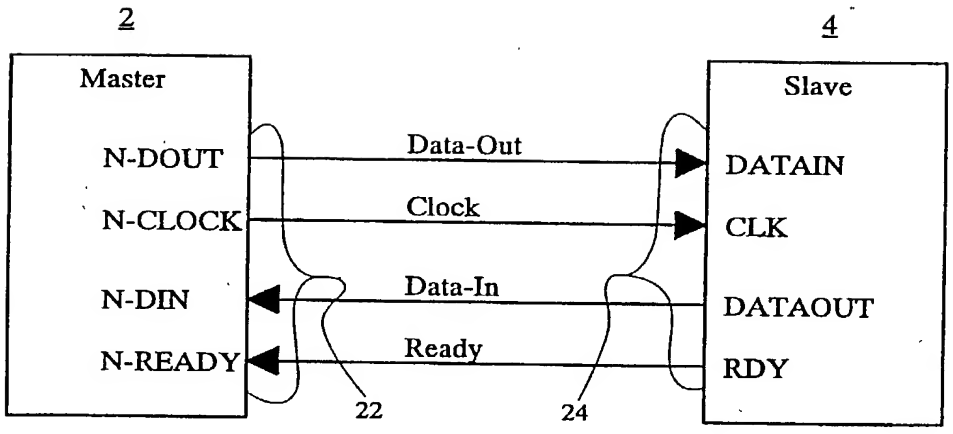
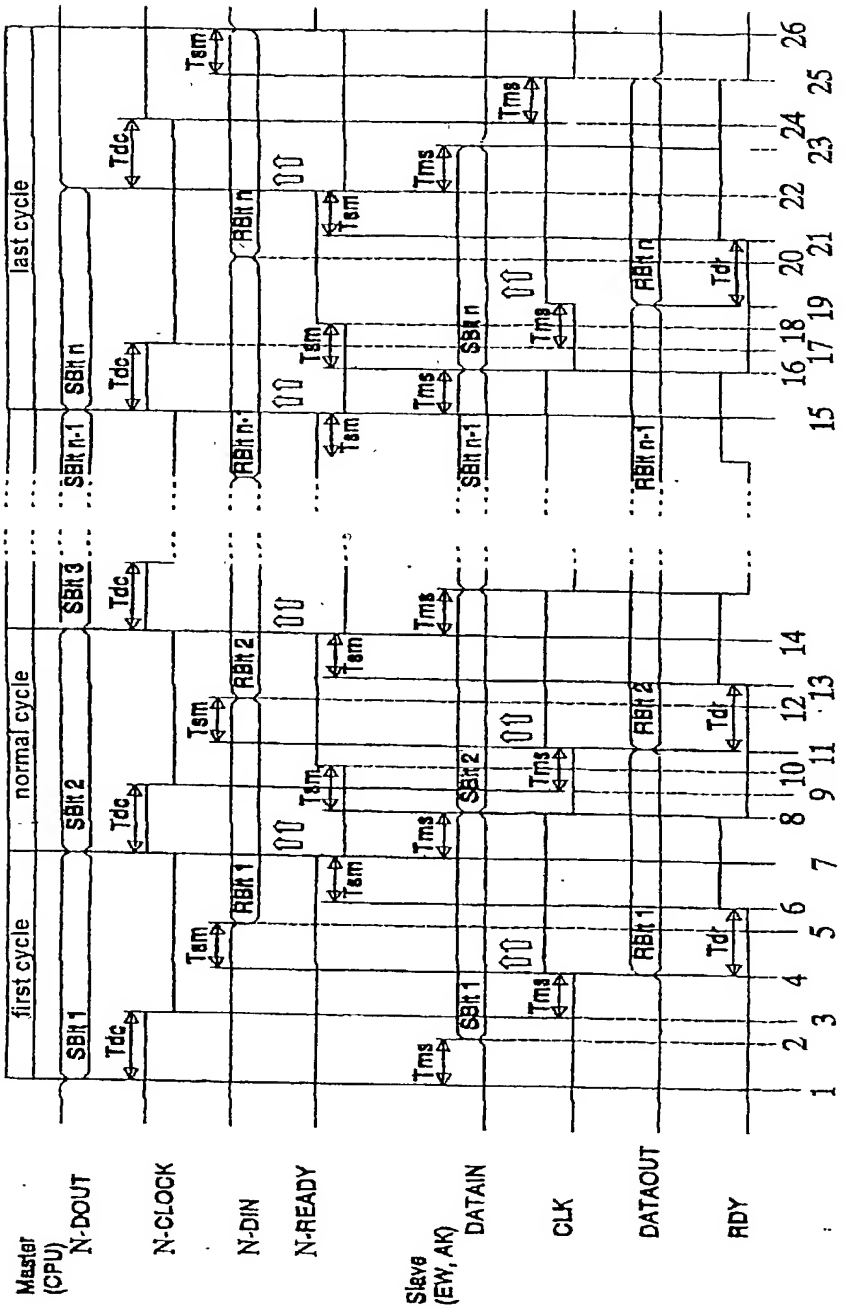

2
Master
N-DOUT
N-CLOCK
N-DIN
N-READY
Data-Out
Clock
Data-In
Ready
22
24
4
Slave
DATAIN
CLK
DATAOUT
RDY

Fig.1

Fig.2


first cycle
normal cycle
last cycle
Master (CPU)
N-DOUT
N-CLOCK
N-DIN
N-READY
Slave (EW, AK)
DATAIN
CLK
DATAOUT
RDY
SBit 1
SBit 2
SBit 3
SBit n-1
SBit n
RBit 1
RBit 2
RBit n-1
RBit n
Tdc
Tsm
Tms
Tdr
1
2
3
4
5
6
7
8
9
10
11
12
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DECLARATION AND POWER OF ATTORNEY

Docket No.. 521.1014

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter that is claimed and for which a patent is sought on the invention entitled:

DATA TRANSMISSION DEVICE

the specification of which (check one)

☐ is attached hereto

☒ was filed on 1 March 2000 as International Application Serial No. PCT/EP00/01745 and was amended on (if applicable).

☒ I hereby authorize and request our attorneys, Davidson, Davidson & Kappel, LLC of 485 Seventh Avenue, New York, New York 10018 to insert here in parentheses (application number 10/070,032, filed 10/18/2001) the filing date and application number of said application when known.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information that is known to me to be material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign and/or provisional application(s) for patent or inventor's certificate listed below and have also identified below any foreign and/or provisional application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR APPLICATION(S)

DE 199 17 576.4 Number	Germany Country	19 April 1999 Day/Month/Year Filed	Priority claimed ☒ Yes ☐ No
Number	Country	Day/Month/Year Filed	Priority claimed ☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial Number	Day/Month/Year Filed	Status
Application Serial Number	Day/Month/Year Filed	Status

And I hereby appoint Clifford M. Davidson, Reg. No. 32,728, Leslye B. Davidson, Reg. No. 38,854, Cary S. Kappel, Reg. No. 36,561, William C. Gehris, Reg. No. 38,156, Morey B. Wildes, Reg. No. 36,968, Robert J. Paradiso, Reg. No. 41,240, Erik R. Swanson, Reg. No. 40,833, Thomas P. Canty, Reg. No. 44,586, and all other registered attorneys and agents at Davidson, Davidson & Kappel, LLC, U.S. Patent and Trademark Office Customer Number 23280, my attorneys, with full power of substitution and revocation, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith; correspondence address: DAVIDSON, DAVIDSON & KAPPEL, LLC, 485 Seventh Avenue, 14th Floor, New York, New York 10018; Telephone: (212) 736-1940; Fax: (212) 736-2427.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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